Stretchable Carbon Nanotube Charge-Trap Floating-Gate Memory and Logic Devices for Wearable Electronics

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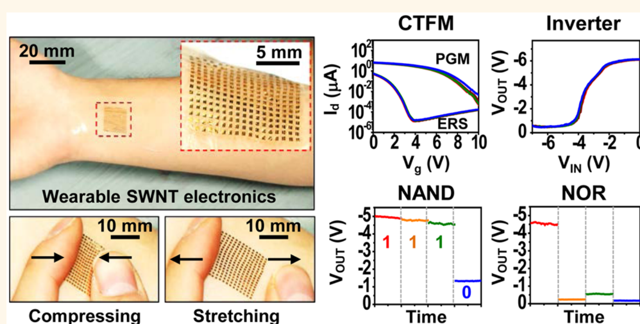
ABSTRACT Electronics for wearable applications require soft, flexible, and stretchable materials and designs to overcome the mechanical mismatch between the human body and devices. A key requirement for such wearable electronics is reliable operation with high performance and robustness during various deformations induced by motions. Here, we present materials and device design strategies for the core elements of wearable electronics, such as transistors, charge-trap floating-gate memory units, and various logic gates, with stretchable form factors. The use of semiconducting carbon nanotube networks designed for integration with charge traps and ultrathin dielectric layers meets the performance requirements as well as reliability, proven by detailed material and electrical characterizations using statistics. Serpentine interconnections and neutral mechanical plane layouts further enhance the deformability required for skin-based systems. Repetitive stretching tests and studies in mechanics corroborate the validity of the current approaches.



KEYWORDS: carbon nanotubes · charge-trap floating-gate memory · logic gates · stretchable electronics · wearable electronics

Along with the increasing interests in wearable electronics, significant advancements have been achieved in technologies for flexible and stretchable devices, such as flexible displays,[1,2] skin-based electronics,[3−6] high-sensitivity deformable sensors,[7−11] wearable human-achine interfaces,[12−14] and compliant energy devices.[15−19] These unconventional electronic, optoelectronic, and energy devices are core components for next-generation wearable electronic systems. Although previous breakthroughs have dramatically advanced related technologies, current electronic devices still suffer from practical problems. One of the most significant concerns is the use of inorganic layers for the active channels and dielectric of conventional electronic devices which may incur mechanical cracks and/or breakdown in repetitive deformations and consequent accumulation of fatigues.[4] The mechanical mismatch between human tissues and inorganic semiconductors aggravates this problem, particularly in skin-based wearable devices.

Extensive research has been conducted to dissipate the induced strain in the channel and active regions, such as ultrathin thickness design approaches,[20] neutral mechanical plane layouts,[21,22] and stretchable interconnections.[23−25] More fundamental changes have been proposed to replace channel materials with soft ones, including graphene[26−28] and carbon nanotubes (CNT).[29−37] Graphene may have issues in terms of the on/off ratio owing to its zero band gap, which is critical for digital circuits. Networks of semiconducting single-walled CNT (s-SWNT) are a promising candidate owing to their potential for high speed/performance electronics by the intrinsically high carrier mobility,[38−43] although challenges in terms of device structures/designs, material optimization, and fabrication/integration

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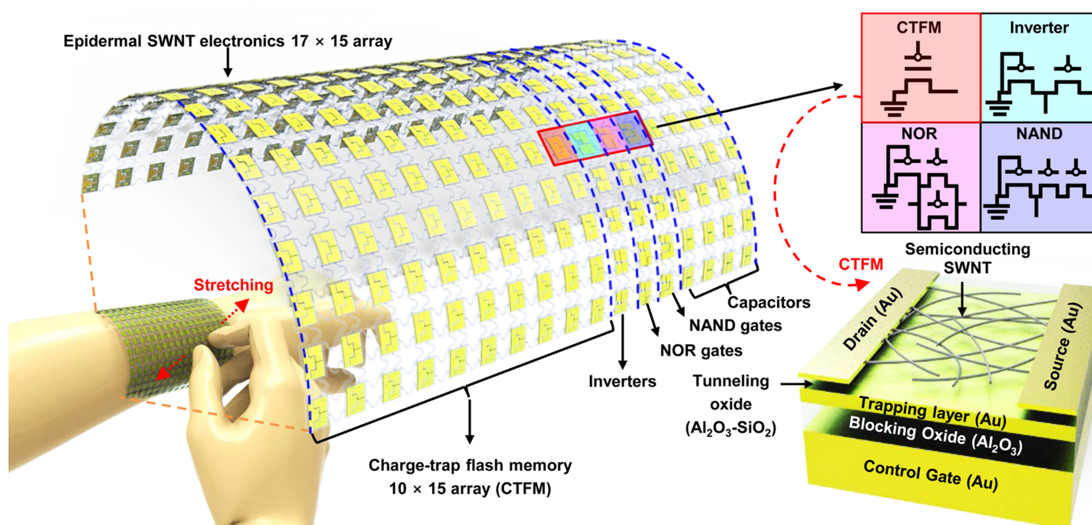

Figure 1. Schematic illustration of the s-SWNT-based electronic devices as a wearable array platform, which consists of memory units, capacitors, and logic circuits (left). Simple circuitry schematics (CTFM, inverter, and NAND/NOR gates) are shown in the top right colored sections. The bottom right frame shows the cross-sectional layer information on the CTFM.

strategies exist. Therefore, efforts to develop stretchable/wearable types of memory modules and other electronic device components for advanced electronic circuits/systems are important. Here, we present materials and device design/fabrication strategies for an array (17 × 15) of s-SWNT-based stretchable electronic devices consisting of capacitors, charge-trap floating-gate memory (CTFM) units, and logic gates (inverters and NAND/NOR gates). Detailed material, electrical, and mechanical characterizations and theoretical analysis in mechanics provide useful insights in the design and development of s-SWNT-based wearable electronic systems.

RESULTS AND DISCUSSION

Figure 1 left depicts a schematic illustration of the wearable array of s-SWNT-based (99.9%-sorted s-SWNT, NanoIntegris Inc., USA) electronic devices composed of capacitors, CTFMs/transistors, and digital circuit components. The circuit diagrams (top) and layer information on the CTFM (bottom) are shown on the right. The ultrathin (<~3 μm) and stretchable system design enables conformal integration of electronics onto the human skin. For mechanical robustness, the entire system is sandwiched between polyimide (PI, Sigma-Aldrich, USA; ~1 μm) ultrathin films. The detailed description of the fabrication processes and an exploded schematic illustration are shown in Figure S1 (Supporting Information), and the corresponding large-scale view in Figure S2. First, a PI layer (~1 μm) is spin-coated on a silicon oxide (SiO_2) wafer, followed by the deposition of Cr/Au (~5 nm/~50 nm) back-gate electrodes using thermal evaporation. All electrodes and charge-trap layers are formed using photolithography and lift-off techniques. After the deposition of a blocking oxide (B_{ox}) layer (~35 nm-thick aluminum oxide (Al_2O_3)) by plasma enhanced atomic layer deposition (PEALD), ~10 nm of gold (Au) is deposited for the charge-trap layer of flash memories. Two consecutive layers of tunneling oxides (Al_2O_3/SiO_2, ~5 nm/~3 nm) are deposited by PEALD (Al_2O_3) and e-beam evaporation (SiO_2). Even though the use of organic dielectric layers would have been advantageous in terms of mechanical flexibility than the chosen inorganic dielectrics, Al_2O_3 is used in this work due to its excellent thickness controllability and uniformity using PEALD, which in turn results in high performance of the CTFM devices. The top surface of SiO_2 is functionalized to form an amine-terminated surface by immersing it into a poly-L-lysine solution (0.1 wt %, aqueous solution; Sigma-Aldrich, USA) for 5 min. Then, random networks of SWNTs (whose average diameter and length are 0.8–1.2 nm and 100–1000 nm, respectively) are deposited by dipping them into an s-SWNT solution (0.01 mg/mL, aqueous solution) for a few hours, followed by thorough rinsing using deionized (DI) water and isopropanol alcohol.[1] After annealing in a globe box at 200 °C for 1 h, isolation of the oxide layers and formation *via* connections follow. The fabrication of the other electronic devices uses similar procedures. But other devices, such as transistors in the logic circuits, do not contain the Au charge-trap layers and fabricated by using different patterns. The entire process is completed by depositing source/drain electrodes (Cr/Au, ~7 nm/70 nm), spin coating the top PI layer (~1 μm), and patterning the final serpentine/island layout by using photolithography and dry etching. Such design of island arrays connected with serpentine-shaped interconnects, with the assist of neutral mechanical plane designs, successfully protected the channel, dielectrics, and contacts during different bending

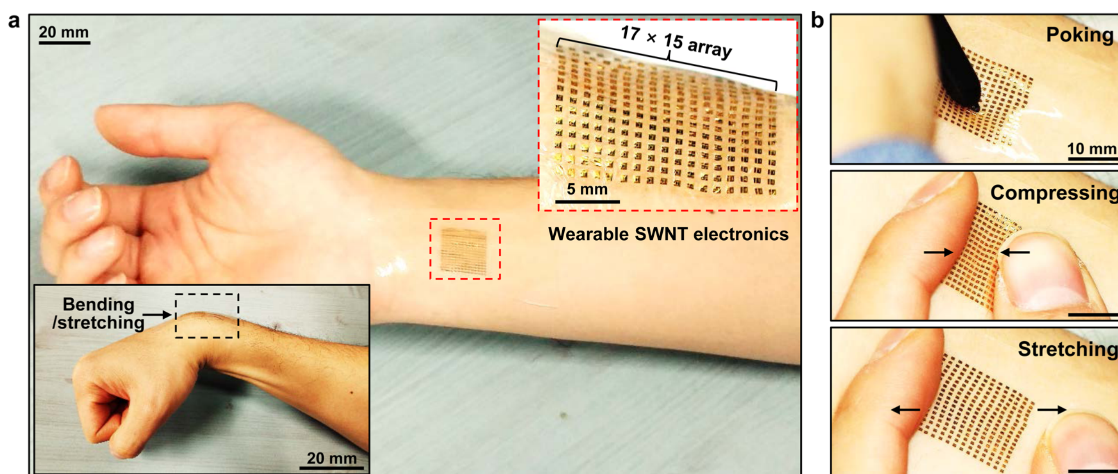

Figure 2. (a) Optical camera image of the array of s-SWNT electronic devices (17 × 15) composed of CTFMs, inverters, NAND/NOR gates, and capacitors. Conformal contacts are well made with a human skin. The insets show a magnified image (top right) and bending/stretching deformations (bottom left). (b) Deformed wearable s-SWNT devices under poking (top), compression (middle), and stretching (bottom).

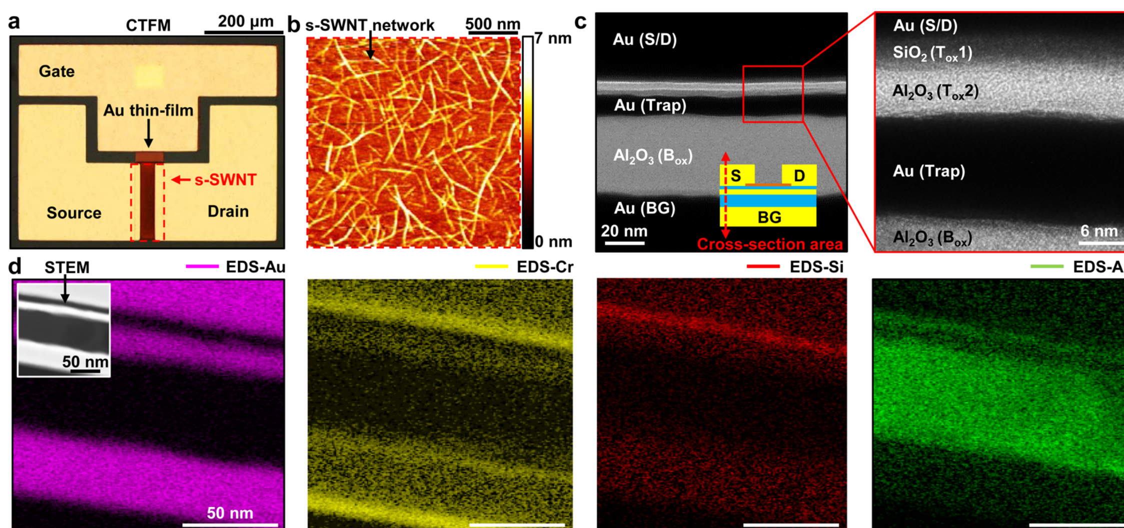

Figure 3. (a) Optical microscope image of a CTFM (top view). The red-dashed box indicates the active channel region composed of a random network of s-SWNTs. (b) AFM image of the 99.9%-sorted s-SWNTs layer showing high density of percolated s-SWNT networks. (c) (left) Cross-sectional TEM image of the CTFM and (right) its magnified view. (d) EDS images showing the elements of each layer: Au, Cr, Si, and Al, from left to right, respectively.

and stretching modes, as will be confirmed later in Figure 8.

Figure 2a represents high-resolution camera images of wearable s-SWNT electronic devices, consisting of CTFMs/transistors (10 × 15 array), inverters (1 × 15 array), NAND/NOR gates (2 × 15 array), and capacitors (4 × 15 array). The inset at the bottom left (black box) shows the conformal lamination on the skin during bending deformations. The inset at the top right (red-dashed box) confirms the conformal contacts of the array through magnified observation. The use of ultrathin PI films with serpentine structures, along with the van der Waals forces, successfully dissipates the induced strains during motions, and maintains intimate contacts. The detailed mechanical and electrical characterizations of these devices under reversible deformations with induced strains (~20%) are discussed later in Figure 8. Further deformations that can possibly occur during daily life activities are shown in Figure 2b. The devices show no delamination and/or mechanical fractures during poking, compression, and stretching (top, middle, and bottom of the figure, respectively).

Figure 3a shows an optical microscope image (top view) of the CTFM with the s-SWNT channel and Au thin-film trap layer. The red-dashed box highlights the active area. The atomic force microscopy (AFM) image shows the magnified view of the s-SWNT networks in the channel (Figure 3b). It has been reported that random networks of SWNTs are well percolated if the density of the connected SWNTs exceeds a certain threshold.[44] This percolation threshold can

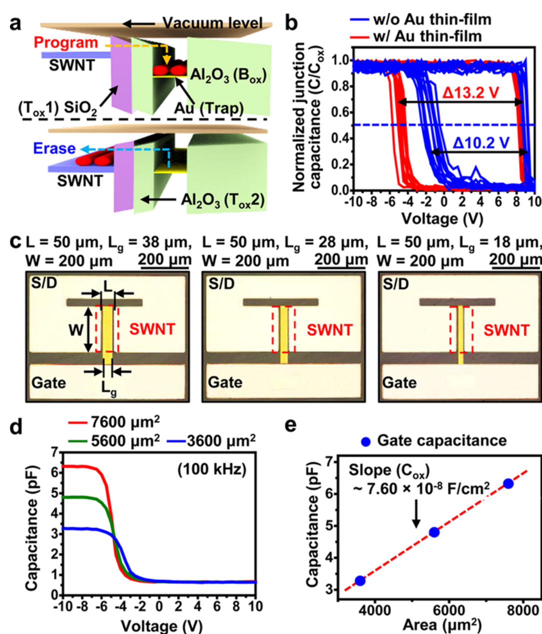

Figure 4. (a) Band bending of the CTFM in the electron charging/discharging process through the T_{ox}1 and T_{ox}2 layers in the PGM/ERS operations. (b) *C*−*V* characteristics showing different voltage hystereses (∼13.2 V with trap layer (red) and ∼10.2 V without trap layer (blue)) with a voltage sweep from −10 to 10 V. (c) Optical microscope images of the nonoverlapped gate/source structures with different gate lengths (L_g) of 38, 28, and 18 μm. (d) Plot of the gate capacitance per unit area. (e) Plot of the capacitance *versus* area with a linear slope (C_{ox}) of ∼7.60 × 10^{-8} F/cm^2.

be approximately quantified by using the number density (per unit area; ρ), in which the average distance between SWNTs, $1/\rho^{1/2}$, equals their average lengths, *i.e.*, $\rho_{th} \sim 1/\langle \text{SWNT length} \rangle^2$. The estimated unit density of the s-SWNT networks is approximately 30−40 tubes/μm^2: given the density, length, and device dimensions (channel lengths of 20, 30, and 40 μm), it can be concluded that the percolation of SWNTs is successfully formed to constitute an electrically conductive path between the source and drain electrodes.[45] Further improvements in the percolation of SWNT networks can be achieved by scaling down the channel length using industry facilities. To understand the structural compositions of the CTFMs, cross-sectional transmission electron microscopy (TEM) and energy-dispersive X-ray spectroscopy (EDS) images are presented in Figure 3c and d, respectively. The magnified TEM image (Figure 3c, right) shows the source/drain (Cr/Au) electrodes (∼7 nm/70 nm), hybrid tunneling oxides composed of ∼3 nm SiO_2 (T_{ox}1) and ∼5 nm Al_2O_3 (T_{ox}2), ∼10 nm Au thin-film trap, and ∼35 nm B_{ox}, from top to bottom. The TEM images of the CTFM show no visible cracks or voids. The elements in each layer are confirmed by EDS data (Figure 3d).

Figure 4a shows two schematic illustrations describing the band bending of the CTFMs under applied positive/negative biases on the gate (program/erase (PGM/ERS) operation of CTFM; top/bottom, respectively). Electrons are trapped in the Au thin-film by tunneling (the band gap of SiO_2 (T_{ox}1) and Al_2O_3 (T_{ox}2) are ∼9 and ∼8.8 eV, respectively) through the ultrathin oxide hybrids (∼3 nm/∼5 nm for $T_{ox}1/T_{ox}2$) under a positive gate bias (PGM operation).[46−48] The ERS operation (negative gate bias) discharges electrons from the Au floating gate to the SWNTs by tunneling through the $T_{ox}1/T_{ox}2$ layers. This charge capturing and releasing behavior of the CTFM is closely related to its junction capacitance, characterized in detail using capacitors. Figure 4b plots the statistical normalized junction capacitance−voltage (*C*−*V*) characteristics (at 2 kHz) with a voltage sweep from −10 to 10 V. A large hysteresis can be observed, which is a well-known phenomenon in SWNT-based devices that mainly results from the hydroxyl groups (−OH) at the interface between the gate dielectric and the SWNTs; the SWNTs in the channel region can be electrostatically modulated by carrier charging and discharging of −OH groups. The *C*−*V* curves with Au thin-film trap (red) exhibit larger hysteresis than that without the trap layer (blue), which proves that the Au thin film serves as a charge-trap layer of the nonvolatile memory unit. The nonoverlapped gate/source structures with different channel lengths/areas (Figure 4c) are used to extract the gate capacitance per unit area (C_{ox}; Figure 4d), while minimizing the parasitic capacitance. A C_{ox} value of ∼7.60 × 10^{-8} F/cm^2 is extracted from the linear slope of the capacitance *versus* area plot (Figure 4e).

The electrical performance of the transistors that compose the CTFMs is characterized under ambient conditions (Figure 5). Figure 5a illustrates the transfer curves (I_d−V_g; drain current-gate voltage) of the transistors in the CTFMs with different channel lengths (*L* = 20, 30, and 40 μm) at the applied drain voltage (V_d) of −5 V. A typical transfer curve of a field-effect transistor (FET, without a charge-trap layer) with *L* = 20 μm is shown in Figure S3, for comparative analysis. Because of the better control of s-SWNTs in the channel area by the gate, the FET exhibits a higher performance in terms of on/off currents. The I_d−V_d and I_d−V_g characteristics of the transistors at *L* = 30 μm under different V_g are shown in Figure S4a and b, respectively. The 150 transistors (10 × 15 array) whose channel lengths (*L*) range from 20 to 40 μm effectively function without significant variations in the on/off ratio and on-current density. Figure 5b shows the cumulated I_d−V_g curves of the 50 transistors in the CTFMs at *L* = 30 μm, exhibiting high device-to-device uniformity. We can further validate these through statistical analysis of the on-current density per unit width (I_{on}/W; Figure 5c), on/off ratio (I_{on}/I_{off}; Figure 5d), transconductance per unit width (g_m/W; Figure 5e), and carrier mobility at V_d = −5 V (μ; Figure 5f). In summary, the averages of I_{on}/W, I_{on}/I_{off}, g_m/W, and μ are 0.36 ± 0.16 μA/μm, >10^5, 0.057 ± 0.021 μS/μm, and 4.51 ± 1.67 cm^2/(V s), respectively. For the estimation of μ, the equation for

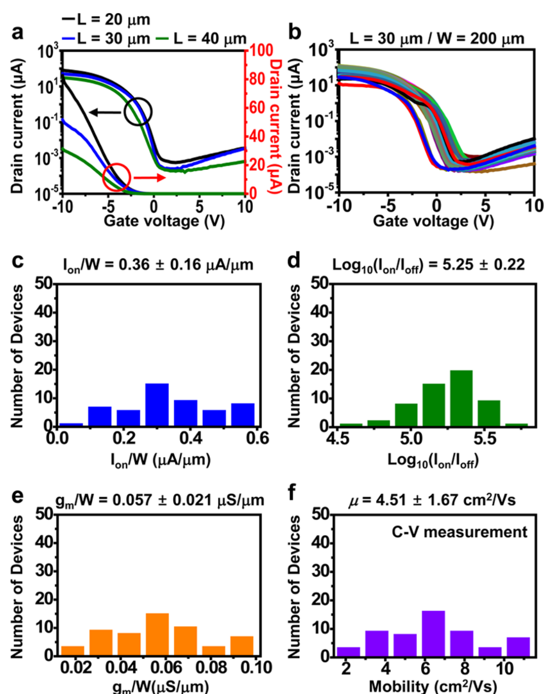

Figure 5. (a) I_d-V_g curves of the transistors that compose the CTFMs with different channel lengths (L = 20, 30, and 40 μm). (b) Cumulative I_d-V_g characteristics of 50 transistors with L = 30 μm. (c) On-current density per unit width at $V_d = -5$ V. (d) On/off ratio at $V_d = -5$ V. (e) Transconductance per unit width at $V_d = -5$ V. (f) Mobility at $V_d = -5$ V.

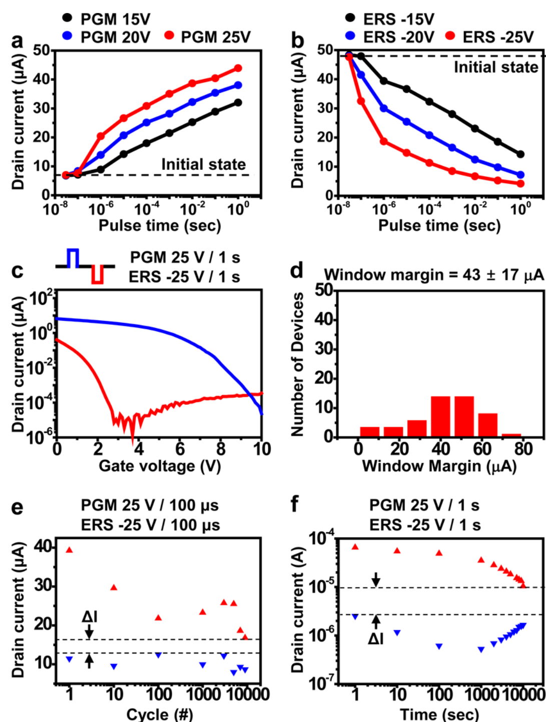

Figure 6. (a) Memory switching characteristics as a function of the pulse time with applied gate voltages of 15, 20, and 25 V for the PGM operation. (b) Memory switching characteristics for the ERS operation with inverse gate voltages of −15, −20, and −25 V. (c) Plot of the two read-out operations. PGM and ERS at +25 and −25 V/1 s, respectively. (d) Statistics of the window margins of the 50 CTFMs after PGM/ERS operations at ±25 V/1 s. (e) Endurance characteristics of the CTFMs during 10 000 PGM/ERS cycles with ±25 V/100 μs. (f) Retention characteristics of the CTFMs under PGM/ERS at ±25 V/1 s.

the parallel-plate model[20] is used, namely, $\mu = Lg_m/(V_dC_{ox}W)$, where C_{ox} = 7.60 × 10^{-8} F/cm^2 (from Figure 4e).

The typical memory switching characteristics of the CTFMs as a function of the pulse time at different gate voltages ranging from ±15 to ±25 V are plotted in Figure 6a and b. The drain current is the current measured at a read voltage of 0 V. For both PGM/ERS operations, increase/decrease in the drain current can be observed even for a short pulse period of 10^{-6}. This result indicates the effective charging/discharging of the carriers into/from the trap layer. Larger change in the drain current can be observed by increasing the duration of the pulse time for both PGM/ERS operations. The CTFM at L = 30 μm is characterized in two read-out PGM and ERS operations at the gate voltage/pulse time of +25 and −25 V/1 s, respectively (Figure 6c). The window margin that corresponds to the difference in the drain current at V_g = 0 and the device-to-device uniformity of the 50 CTFMs are appropriate for unambiguous read-out (Figure 6d). Figure 6e shows the endurance characteristics of the CTFMs under the operating condition of ±25 V/100 μs. The CTFMs maintain substantial window margins even after PGM/ERS operations of 10 000 cycles. The retention test (Figure 6f) also verifies the reasonable window margin maintained after approximately 10 000 s.

In addition to the capacitors, transistors, and CTFMs, logic gates are important components in digital circuits. The voltage transfer curves (VTCs) and output characteristics of the logic gates (inverters and NAND/NOR gates) are shown in Figure 7. An optical microscope image of an inverter and its VTCs (V_{DD} ranging from −5 to −10 V) are shown in Figure 7a and b, respectively. The VTCs show typical input/output behavior of the logic inverter; *i.e.*, V_{OUT} decreases from 0 to V_{DD} as V_{IN} increases from V_{DD} to 0. The voltage gains at each V_{DD} are shown in Figure 7c and their summary is shown in Figure 7d (top). An important factor in the characterization of inverter performance is the noise margins, *i.e.*, the high- and low-state noise margins (NM_H and NM_L). NM_H and NM_L are estimated as $NM_H = V_{OH} - V_{IH}$ and $NM_L = V_{IL} - V_{OL}$, where V_{OH}, V_{OL}, V_{IH}, and V_{IL} denote the output high voltage, output low voltage, input high voltage, and input low voltage, respectively. The measured noise margins with respect to different V_{DD} are plotted at the bottom of Figure 7d. The detailed values are listed in Table S1. The average noise margin for the applied V_{DD} is 0.190 × V_{DD}, which shows the reliable and robust operation of the inverters. The inverter is successfully extended for more advanced logic gates (two-input NAND and NOR; Figure 7e and g), as shown in their output characteristics (Figure 7f and h). V_{DD}

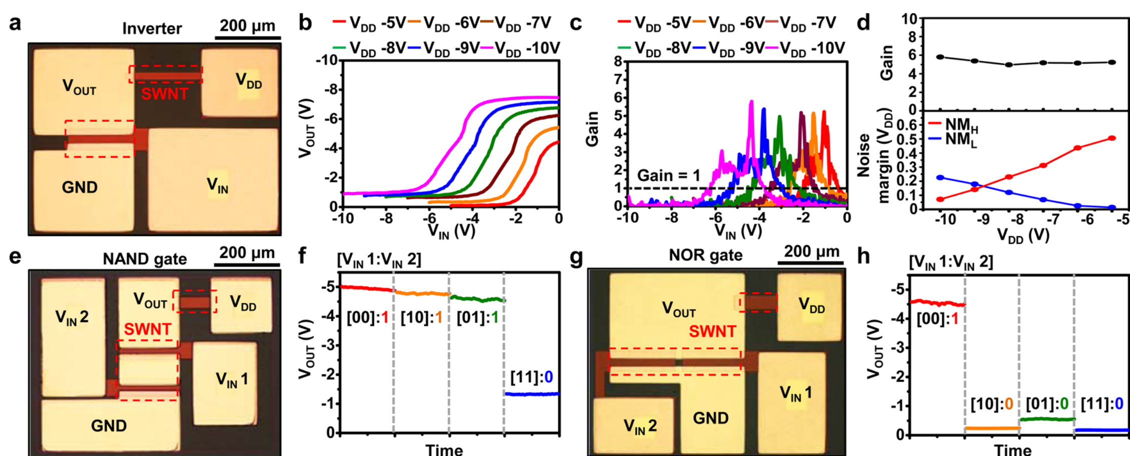

Figure 7. (a) Optical microscope image of an inverter. The red-dashed box indicates the random network of s-SWNTs in the active channel region. (b) VTCs showing the input and output behavior of the inverter. V_{DD} varies from −5 to −10 V. (c) Voltage gain of the inverter. (d) (top) Summary of voltage gains and (bottom) noise margins with respect to different V_{DD} ranging from −5 to −10 V. (e) Optical microscope image of a two-input NAND logic gate. (f) Output characteristics of a two-input NAND logic gate with V_{DD} of −5 V and input voltages of −5 and 0 V. (g) Optical microscope image of a two-input NOR logic gate. (h) Output characteristics of a two-input NOR logic gate with V_{DD} of −5 V and input voltages of −5 and 0 V.

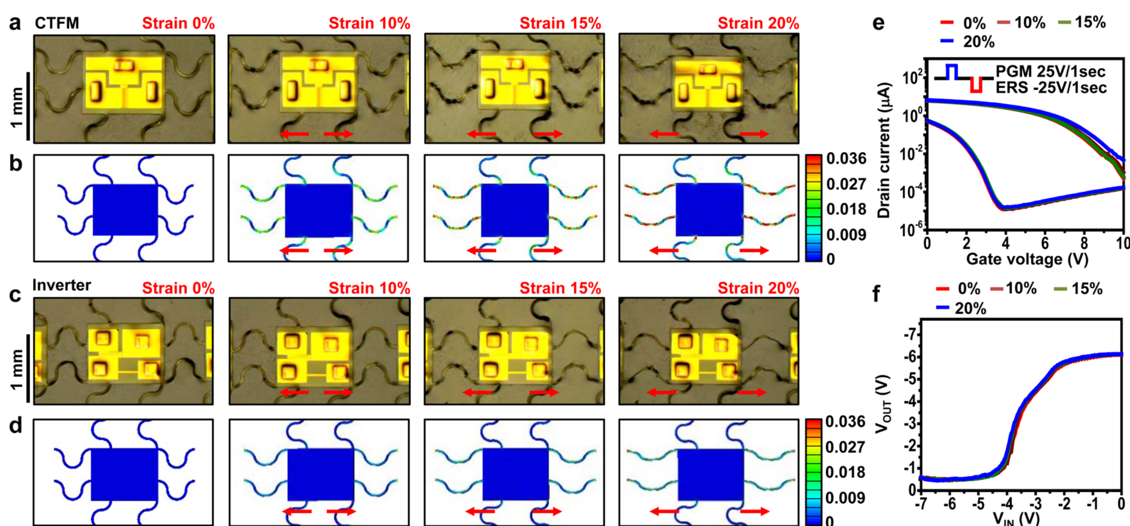

Figure 8. (a) Optical microscope image and (b) FEA strain distribution results of the CTFM under applied strains between 0 and 20%. The red arrows indicate the strain direction. (c) Optical microscope image and (d) FEA strain distribution results of the inverter under applied strains between 0 and 20%. (e) Electrical characteristics of the CTFM under applied strains between 0 and 20% (PGM and ERS at −25 and +25 V/1 s, respectively). (f) VTCs of the inverter showing stable operation under applied strains between 0 and 20%.

of −5 V is used along with input voltages of −5 and 0 V for logic "1" and "0", respectively.

In wearable electronics, a stable electrical operation of devices under external applied strains is important. The electrical performance results of s-SWNT CTFMs and inverters with different uniaxial strains (up to ∼20%; typical maximum strain induced in a human skin[5]) are characterized and compared with theoretical analyses, as shown in Figure 8. The island-shape active and serpentine-shape interconnection designs, together with the neutral mechanical plane layout,[16] enable the devices to endure an ∼20% applied strain while minimizing the deformations/strains in the channels and active regions (Figure 8a and c; see strain distributions obtained by Finite Element Analysis (FEA) under each applied strain in Figure 8c and d). It can also be inferred that the disconnection issues of SWNT network percolations and/or extraction of SWNTs from the metal source/drain contacts is effectively avoided by unwanted movements of the SWNTs due to the applied strain. The maximum induced strain in the active (∼0.001) and interconnection (∼0.036) regions is below the typical fracture strain of the device components. The corresponding electrical characterizations of the CTFMs and inverters during the stretching tests are shown in Figure 8e and f, respectively. The PGM and ERS curves of the CTFM (PGM and ERS at +25 V/1 s and −25 V/1 s) and VTCs of the inverter under external strains show no visible variations and/or signs of electrical degradations. Even after stretching

for 1000 times with ~20% applied strain, the device performance shows minimal changes (Figure S5). In addition, the bending test of the inverter is conducted at different radii of curvature between infinite (flat) and ~5 mm bending radii (Figure S6a). The induced strains on the inverter (FEA; Figure S6b) are negligible. The stable electrical characterization results confirm the effectiveness of the material and design strategies (Figure S6c).

CONCLUSION

In summary, we have reported stretchable s-SWNT-based electronic devices, such as capacitors, transistors, nonvolatile memory units, and logic gates. The arrayed stretchable devices are conformally laminated on a curvilinear and soft human skin. Deformations including poking, compression, and stretching do not cause delamination or mechanical fractures. The detailed material analyses using electron and elemental microscopies as well as the theoretical explanations based on numerical mechanic modeling/simulations validate the electrical characterizations, *i.e.*, the reliable device operations. The performance of the memory and logic devices is well maintained even after repetitive stretching/fatigue tests. These soft electronic devices based on s-SWNTs can provide novel opportunities for wearable electronics.

METHODS

Fabrication of s-SWNT-Based Wearable Electronic Devices. The detailed fabrication processes and materials used in the devices are described in the Results and Discussion section, supplemented by Figures 1, S1, and S2. Before the devices are transferred onto a human skin, the entire system is picked up from an SiO_2 temporary supporting substrate using water-soluble tape (3M, USA) and transferred onto a thin layer of polydimethylsiloxane ((PDMS), Dow Corning, USA). The water-soluble tape is dissolved using DI water to release the devices, which are subsequently transfer-printed on the skin.

Characterization of the Device Structures. The top-view images of the CTFMs, inverters, NAND/NOR gates, and capacitors are captured using an optical microscope (BX51 M, Olympus, USA). The density of the s-SWNT networks is examined using an atomic force microscope (Dimension Icon, Bruker, UK). The TEM images and the corresponding EDS data are taken using an electron microscope (JEM-2010, JEOL, Japan) operated at an acceleration voltage of 200 kV. For the cross-sectional analysis, the samples are cut using a focused ion beam (Quanta 3D FEG, FEI, USA) in the channel/trap region.

Characterization of the Electrical Properties. The $C-V$ measurements are conducted at a 100-kHz frequency at ±10 V using a parameter analyzer (B1500A, Agilent, USA) equipped with an LCR meter and a probe station (MSTECH, Republic of Korea). The $I-V$ curves are obtained using the same setup. The stretching tests are conducted using an automatic stretching stage that applies compressive and tensile strains in the x and y directions.

FEA of the CTFMs and Inverters. Finite element simulations are used to analyze the strain distribution of the CTFMs and inverters during the stretching (Figure 8b and d) and bending tests (Figure S6b). The CTFMs and inverters are modeled using four-node composite shell elements. The devices/substrates are modeled using eight-node solid elements. We assume perfect bonding (no-slip condition) between the devices and substrates. To simulate stretching, stretching boundary conditions are applied at the bottom surface of the substrate. To simulate bending, rotation boundary conditions corresponding to the given radius of curvature are applied at the bottom of the substrate. The isotropic linear elasticity represents the behavior of the materials of the flash memory devices and inverters. The Young's moduli of the CNT, Au, Al_2O_3, SiO_2, and PI are 1 TPa, 77.2, 463, 73.1, and 2.5 GPa, respectively. The Poisson's ratios of CNT, Au, Al_2O_3, SiO_2, and PI are 0.22, 0.42, 0.22, 0.17, and 0.34, respectively. The incompressible neo-Hookean model is used to represent the substrate: $W = C_1 (I_1 - 3)$ where W is the strain energy potential, I_1 is the first invariant of the left Cauchy−Green tensor, and C_1 (=3 kPa for the PDMS substrate) is a material parameter.

Conflict of Interest: The authors declare no competing financial interest.

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Supporting Information Available: The fabrication process, I_d-V_d output curves, transfer curves under different V_g, VTCs of the inverters after cycled stretching tests and bending tests are included. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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